REMARKS

Pursuant to the Examiner's request, to supplement the response filed on December 9, 2005, Applicants submit this Supplemental Amendment. The above amendments to the specification are identical to the amendments in Amendment A, filed on May 28, 2003 (a copy of which was resubmitted with the U.S. Patent and Trademark Office on September 9, 2003 and August 6, 2004). However, the amendments to the specification contained herewith have been underlined pursuant to the Examiner's request to make the amendments compliant.

In addition, the Examiner requested that the Supplemental Declaration filed on December 9, 2005 be corrected to include the Amendment date of August 6, 2004. However, no new amendment was filed on August 6, 2004. A copy of Amendment A of May 28, 2003 was submitted on August 6, 2004. The Amendment date of May 28, 2003 is listed on the Supplemental Declaration. Therefore, Applicants submit that the Supplemental Declaration filed on December 9, 2005 is complete.

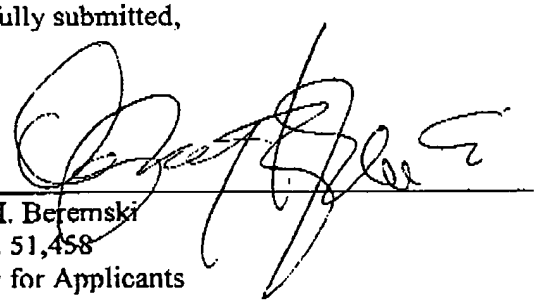
Furthermore, the Examiner requested a copy of the Preliminary Amendment, filed on July 21, 2000 with the initial filing of the application, for part of the Preliminary Amendment is missing from the U.S. Patent and Trademark Office's records. A copy of the Preliminary Amendment of July 21, 2000 is enclosed. Pursuant to the Preliminary Amendment of July 21, 2000, the Applicants have cancelled claims 1-33 and 41-144.

In view of the above amendments and remarks, Applicants believe that this application is in condition for allowance.

The Commissioner is hereby authorized to charge any additional required fees or credit any over payment by this submission to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: December 16, 2005

Respectfully submitted,



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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EXPRESS MAIL NO. EL 488178705US

Applicant : Henry Samueli, et al
Filed : Herewith
Title : ETHERNET SYSTEM

Docket No. : 39966/LTR/B600

PRELIMINARY AMENDMENT

Post Office Box 7068
Pasadena, CA 91109-7068
July 21, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

Commissioner:

Please amend the above newly filed continuation application as follows:

In the Specification:

Please insert

-- CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of allowed Application No. 09/252,551 filed February 18, 1999, which was a reissue of Patent No. 5,604,741 issued February 18, 1997, the disclosures of which are incorporated fully herein by reference. --

Page 6, line 37, delete "megabauds" and insert -- megasymbols -- and delete "Mbaud/sec" and insert -- Msymbol/sec --.

Page 9, line 57, delete "baud" and insert -- symbol --.

Page 10, line 3, delete "baud" and insert -- symbol --;
line 29, delete "baud" and insert -- symbol --;
line 32, delete "baud" and insert -- symbol --;

line 42, delete "baud" and insert -- symbol --;
line 50, delete "baud" and insert -- symbol --;
line 52, delete "baud" and insert -- symbol --;
line 54, delete "baud" and insert -- symbol --;
line 59, delete "baud" and insert -- symbol --;
line 64, delete "baud" and insert -- symbol --;

line 66, delete "baud" and insert -- symbol --.

Page 11, line 2, delete "baud" and insert -- symbol --;
line 15 and 16, delete "baud" and insert -- symbol --;
line 30, delete "baud" and insert -- symbol --;
line 44, delete "baud" and insert -- symbol --.

Page 12, line 65, delete "baud" and insert -- symbol --.

Page 13, line 33, delete "baud" and insert -- symbol --.

In the Claims:

CANCEL CLAIMS 1-33 AND 41-144

Add the following new claims:

-- 145. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter for digitally converting the multi-level signal at a particular rate;

a timing recovery circuit for regulating the particular rate at which said analog to digital converter converts the multi-level signal; and,

a digital adaptive equalizer for receiving the digitally converted multi-level signal and selecting one of a plurality of levels. --

-- 146. The apparatus of claim 145, further comprising an automatic gain control circuit coupled to said analog to digital converter. --

-- 147. The apparatus of claim 145, further comprising a decoder circuit coupled to said digital adaptive equalizer. --

-- 148. The apparatus of claim 147, further comprising a media access controller coupled to said decoder circuit. --

-- 149. The apparatus of claim 145, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer. --

-- 150. The apparatus of claim 145, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples. --

-- 151. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal transmitted at a transmission rate of at least 25 megasymbols per second, comprising:

an analog to digital converter that is responsive to the multi-level signal transmitted at the transmission rate of at least 25 megasymbols per second;

a clock recovery circuit coupled to said analog to digital converter; and,

a digital adaptive equalizer coupled to said analog to digital converter. --

-- 152. The apparatus of claim 151, further comprising an automatic gain control circuit coupled to said analog to digital converter. --

-- 153. The apparatus of claim 151, further comprising a decoder circuit coupled to said digital adaptive equalizer. --

-- 154. The apparatus of claim 153, further comprising a media access controller coupled to said decoder circuit. --

-- 155. The apparatus of claim 151, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer. --

-- 156. The apparatus of claim 151, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples. --

-- 157. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter;

a clock recovery circuit coupled to said analog to digital converter; and,

a digital adaptive equalizer coupled to said analog to digital converter. --

-- 158. The apparatus of claim 157, further comprising an automatic gain control circuit coupled to said analog to digital converter. --

-- 159. The apparatus of claim 157, further comprising a decoder circuit coupled to said digital adaptive equalizer. --

-- 160. The apparatus of claim 159, further comprising a media access controller coupled to said decoder circuit. --

-- 161. The apparatus of claim 157, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer. --

-- 162. The apparatus of claim 157, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples. --

-- 163. A method for recovering a multi-level signal transmitted on at least one pair of twisted wires, comprising:

converting the multi-level signal to a digital signal at a particular rate;

regulating the particular rate of conversion;

equalizing the digital signal; and,

selecting one of a plurality of levels based on the digital signal. --

-- 164. The method of claim 163, wherein the particular rate is regulated in accordance with a product of a plurality of peak signal samples. --

-- 165. The method of claim 163, wherein the particular rate is at least 25 megasymbols per second. --

-- 166. The method of claim 163, decoding the selected level. --

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

LeRoy T. Rahn
Reg. No. 20,356
626/795-9900

LTR/dg
DLG PAS2G3286 1-*-7/31/00 3:31 PM